[redacted]

27. A method of pre-computing routes for nets in a region of an integrated circuit ("IC") layout, the method comprising:

a) defining a set of partitioning lines for partitioning the region into a plurality of sub-regions during a routing operation;

b) for a set of potential sub-regions, identifying a set of routes that traverse the potential set of sub-regions, wherein at least one of the routes has at least one diagonal edge; and

c) storing the identified routes.

28. The method of claim 27, wherein a plurality of paths exist between the sub-regions defined by the set of partitioning lines, wherein a plurality of the paths are diagonal paths, wherein at least one of the routes traverses some of the diagonal paths.

29. The method of claim 28 wherein identifying the routes comprises identifying the paths between the sub-regions used by each route.

30. The method of claim 29, wherein a plurality of the paths are Manhattan paths, wherein at least one of the routes traverses some of the Manhattan paths.

31. The method of claim 27, wherein a plurality of edges exist between the sub-regions defined by the set of partitioning lines, wherein a plurality of the edges between the sub-regions are diagonal edges, wherein at least one of the routes intersects at least one of the diagonal edges.

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32. The method of claim 31, wherein identifying the routes comprises identifying the edges between the sub-regions intersected by each route.

33. The method of claim 32, wherein a plurality of the edges between the sub-regions are Manhattan edges, wherein at least one of the routes intersects at least one of the Manhattan edges.

34. The method of claim 33 further comprising:

a) for each particular set of potential sub-regions from a group of potential-sub-region sets, identifying a set of routes that traverse the particular set of potential sub-regions, wherein some of the routes have diagonal edges; and

b) storing the identified routes.

35. The method of claim 34, wherein the group of sets includes all possible sets of sub-regions including sets with zero or one sub-region, wherein the identified sets of routes for sets of sub-regions with zero or one sub-region are empty.

36. The method of claim 34, wherein the group of sets includes all combinations of two or more sub-regions.

37. For a router that uses a set of partitioning lines to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions, wherein a plurality of routing paths exist between the sub-regions, a method of pre-computing routes for connecting said sub-regions, the method comprising:

[redacted]

for each particular combination of two or more sub-regions, identifying at least one route for connecting the particular combination of said sub-regions;

identifying the routing paths used by each identified route, wherein some of the identified routing paths are diagonal; and

storing the identified routing paths for each identified routes in a storage structure.

38. The method of claim 37, wherein some of the routing paths are horizontal.

39. The method of claim 37, wherein some of the routing paths are Manhattan.

40. The method of claim 39, wherein the Manhattan routing paths are defined with respect to a first grid, and wherein the diagonal routing paths are defined with respect to a second grid.

41. The method of claim 37, wherein the set of partitioning lines includes intersecting lines that form a partitioning grid.

42. For a router that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of edges exist between said slots, a method of pre-computing routes for connecting said sub-regions, the method comprising:

for each particular combination of at least two of said slots,

identifying at least one routing graph for connecting the particular combination of said slots;

identifying the edges intersected by each routing graph identified for the particular combination of said slots,

wherein some of the identified edges are diagonal; and

storing the identified edges for each routing graph identified for the particular combination of said slots in a storage structure.

43. The method of claim 42, wherein some of the edges are horizontal.

44. The method of claim 42, wherein some of the edges are Manhattan.

45. The method of claim 44, wherein the Manhattan edges are defined with respect to a first grid, and wherein the diagonal edges are defined with respect to a second grid.

IN THE ABSTRACT

On page 175, lines 1-8, please delete the "Abstract of the Invention", and insert therein a new Abstract of the Invention as follows: